Comments on Final Draft of Version 2.0 of Energy Star Eligibility Criteria for EPS from STMicroelectronics.

Dear Sirs,

Here below you can find the comments from STMicroelectronics on the final draft of version 2.0 of Energy Star eligibility criteria for External Power Supplies (EPS).

Although in this final draft version the need for differentiating the **efficiency requirements versus the output voltage** was recognized, it is our opinion that it is not yet fully satisfactory.

The efficiency loss due the voltage drop V_F across the secondary rectifier(s) in an EPS with an output voltage Vout is V_F/Vout, almost regardless of its nameplate output power. Since Energy Star program covers applications whose output voltage may range from 5V (such as in cellular phone adapters) to 30+ V (such as in printer adapter), whatever level of V_F is considered the efficiency loss may change by a factor of 30 / 5 = 6 or more (e.g., with V_F=0.5 V the efficiency loss would be 10% in a 5V output application and 1.7% in a 30V output application). One more point needs to be considered: the efficiency is to be measured with the output cable in place, then the relevant losses need to be considered as well. With the same output power level, the output current is inversely proportional to Vout and cable losses are proportional to the squared current, then the efficiency loss on the output cable would be proportional to $1/Vout^2$. To contain this loss, an increase of copper usage is needed, which is definitely not in favor of the present and highly welcome "green power" trend.

This considering, **a single voltage divide (6V) and 1% efficiency requirement gap both appear too low**. Although an efficiency formula that includes Vout in addition to P_{no} would be desirable, we recognize that this might not be an easy task to do.

An additional comment concerns the **0.9 power factor requirement**.

In our view, whereas this makes much sense in Japan or US power distribution lines where the low input voltage causes a larger input current and where, consequently, the effect of a low power factor is an important contributor to the conduction losses in distribution wiring, this is less significant in the European mains. As compared to the US mains, with the same power throughput the current is half and the conduction loss is one fourth. One more point is worth

attention in our opinion: the power factor always degrades as the line voltage increases. There are many reasons for that, but in the Pareto distribution the major contributor is the displacement current drawn by the so-called Cx capacitors. These capacitors are connected between phase and neutral and are part of the differential mode input filter that is required to comply with EMC regulations. They draw a current proportional to the squared rms line voltage that leads by 90 degrees the instantaneous line voltage. This, even with an undistorted current absorption, will degrade the power factor regardless of how efficiently the power stage handles the throughput power.

Regardless of the mains voltage, to improve power quality it is probably more important to mitigate the harmonic current emissions rather than achieving a higher power factor, as testified by the well-consolidated EN61000-3-2 and JIS C 61000-3-2 regulations.

One objection to harmonizing the Energy Star 2.0 requirements to these world-wide used references is that there are no limits assigned for the US mains. This is actually a minor obstacle if one notices that the limits of JIS regulations are derived from those of the EN regulations by simply multiplying the EN limits by 2.3, ratio of the respective nominal mains voltages. **The limits for the US mains would be then found by simply doubling the EN limits.** By experience, for US mains, complying with these limits would almost inevitably lead to a power factor > 0.9.

A final comment concerns the **efficiency target for low power applications**.

In the $P_{no} \leq 5$ W range the application that is by far dominant is the cellular phone charger. Based on typical charging profiles (**the charger runs at power over 25% of its nameplate value for a very limited time as compared to that when it operates with no load**), many case studies show that the energy saving resulting from the efficiency increase is almost negligible if compared to the energy saving resulting from even not much tighter no-load requirements. Then, it is STMicroelectronics opinion that **for this class of applications increasing the minimum average active mode efficiency is of little use.**

To summarize, STMicroelectronics would like to suggest the followings:

1) To split the active mode efficiency requirements in three classes (Vout < 6V, 6V≤ Vout ≤ 15V, Vout>15V) with max. targets at P_{no} >49 W of 80%, 84% and 87% respectively.
2) To leave the same efficiency targets as in Energy Star 1.0 for applications P_{no}≤ 5 W, regardless of Vout and then adapting the progressive formulae of efficiency vs. P_{no} depending on the Vout class, so as to achieve the maximum values at P_{no} >49 W as above specified.
3) To decrease the no-load input power requirement for applications P_{no}≤ 5 W to 0.2W, regardless of the output voltage.
4) To eliminate the power factor requirement and harmonize the Energy Star 2.0 power quality requirements to EN61000-3-2 Class D with an obvious change of the harmonic current limits due to the different mains voltage.

Sincerely,

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